EFFECTS OF SUBSTRATE MATERIAL AND PACKAGE PAD DESIGN ON SOLDER-JOINT RELIABILITY OF 0.8MM PITCH BGA

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ABSTRACT
This paper describes experimental work to improve the solder-joint reliability (SJR) of a 0.8mm pitch, 25mm body BGA (ball grid array) package used in automotive under-the-hood applications. Testing was TCoB (temperature cycle on board) in AATS (air-to-air thermal shock) between -40°C and +125°C. The target requirement was to pass 3000 cycles before the first failure.

A six-cell experimental matrix was run to study the impact of two variables: substrate dielectric material and package pad design type. Two-parameter Weibull curves were fit to the data from each cell, and regression analyses performed on the characteristic lives derived from those fits. Results showed that lowering the substrate dielectric CTE (coefficient of thermal expansion) improved characteristic life 22%. Also, a package design hybrid of SMD (soldermask defined) and NSMD (non-soldermask defined) pads improved characteristic life 30% compared to a pure SMD design.

The improvement observed by lowering substrate CTE has been attributed to the reduction in package warpage by more closely matching the substrate and mold compound CTEs. The hybrid design improvements resulted by strategically choosing the NSMD sites, altering the distribution of solder-joint cracking within the BGA array.

Either improvement was able to delay first failure beyond 4000 cycles, meeting the target requirements. Together, these changes drove the first failure to 5000 cycles.

INTRODUCTION
The automotive industry continues to drive increased SJR (solder-joint reliability) for under-the-hood applications. One aspect of SJR, TCoB (temperature cycle on board) assesses thermal fatigue resistance of solder interconnection between component and PCB (printed circuit board) during temperature excursions. In some instances, requirements on number of cycles to first failure have increased 2x over previous product generations.

It has been long established that packages using NSMD BGA pads were more resilient than ones with SMD pads to fatigue induced solder-joint cracks [1, 2]. However, NSMD pads in our previous investigations on 292MAPBGA and 416PBGA packages failed sooner in AATS testing due to an alternate failure mode: substrate Cu trace cracks [3]. Detailed failure analysis revealed that these cracks occurred exclusively on BGA pads in the die shadow. This led to the idea that a mixed design – NSMD pads outside the die shadow, while maintaining SMD pads under the die – could perform better than a pure SMD design.

Separately, lower CTE (coefficient of thermal expansion) substrate dielectric materials were under investigation as a means to reduce package warpage. Below Tg, the mold compound CTE is 9ppm/°C. The standard substrate dielectric CTE is 16ppm/°C, resulting in considerable package warpage at lower temperatures. It was hypothesized that lowering the substrate dielectric material CTE to 11ppm/°C would reduce package warpage which in turn should reduce solder-joint strain thereby increasing solder-joint lifetime.

A six-cell experimental matrix was run to study the impact of these two variables (substrate dielectric material and package pad design type.) These experiments used standard daisy-chain temperature cycle testing methodology. Assemblies were monitored in situ to detect failures as they occurred, and 2-parameter Weibull failure distributions were fit to the data. Various metrics derived from the Weibull fits were regressed against the DOE variables to determine which had significant impact on solder-joint lifetime, and to what degree. Crack growth was assessed using cross-section and dye-and-pry techniques on unmonitored assemblies that were removed from the chambers at fixed readpoints. Conclusions on the impact of the parameters were determined based on the totality of electrical test and crack growth data.

EXPERIMENTAL
Design
The package attributes are summarized in Table 1. Those highlighted in yellow were varied in the experiment. The substrate dielectric details are in Table 2. BGA arrays are shown in Figure 1. The baseline SMD design in Figure 1a contained only SMD pads. Hybrid-A in Figure 1b used the same footprint, but the outer four rings were substituted with NSMD pads, while the pads at the die edge were maintained as SMD. By contrast, the outer six rings were NSMD for Hybrid-B, encompassing the die edge. In all cases, the SMD pad SRO (solder resist opening) was 0.45mm. To compensate for solder wetting down the pad

sidewall, the NSMD pads on the hybrid designs were slightly smaller in order to produce a similar ball height.

These packages were daisy-chain test vehicles with pairs of solder-joints electrically connected as illustrated in Figure 2. A complete circuit was created by connecting pairs on the PCB side that were skipped on the package. All solder-joints were monitored as one "net". A failure on any solder-joint meant the remaining solder-joints could no longer be electrically monitored.

Except where parameters were intentionally varied, the daisy-chain packages were mechanically similar to the final products: same die size, area and thickness. Similarly, the same material sets were used: mold compound, die attach, and assembly factory.

Table 1: Package details. DOE variables in yellow.

Parameter	512TEPBGA
Body Size	25mm x 25mm
BGA Pitch	0.8mm
Mold Size	22.5mm x 22.5mm
Mold Thickness	1.15mm
Mold Material	Epoxy Mold Compound α1=9ppm/°C E=26GPa Tg=125°C (TMA)
Substrate Thickness	0.56mm, 4 layer
Substrate Material	Variable – See Table 2
Die Size	8.1mm x 9.6mm x 0.28mm
Package Pad Design	Variable – See Figure 1
Package SRO	0.45mm
Pad Finish	Electroplated Ni/Au
Sphere Diameter	0.50mm
Sphere Alloy	Sn 3.5Ag

Table 2: Substrate dielectric mechanical properties.

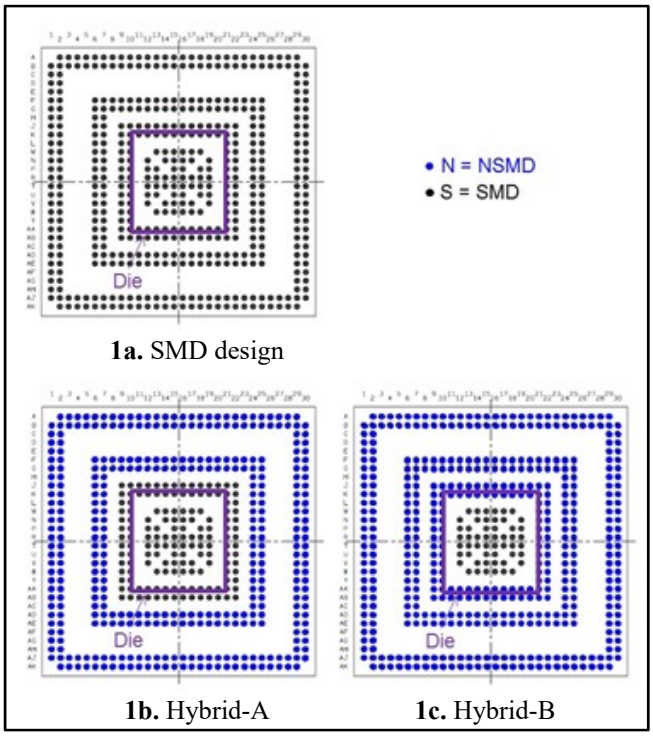
Substrate Dielectric	CTE (TMA)	Modulus (DMA)	Tg (TMA)
Standard	α1=16ppm/°C	19GPa	180°C
Low CTE	α1=11ppm/°C	22GPa	260°C

Assembly

The PCB and assembly details are in Table 3. Assembly of daisy-chain parts to boards followed industry norms. Solder paste printed to boards used the alloy Sn3.8%Ag0.7%Cu (SAC387) and a no-clean flux system. Placement of parts to boards used a dual eyepiece placement machine for aligning parts to solder-paste print. Finally, boards were run through a 10-zone reflow furnace with a peak temperature between 235°C and 245°C.

Experimental Matrix

The six experimental cell combinations shown in Table 4 were built and tested. 16 from each were subjected to monitored TCoB -40°C/+125°C cycling, with additional unmonitored units included for crack propagation measurements. Non-destructive T0 characterization was performed on all cells.



1a. SMD design

1b. Hybrid-A **1c.** Hybrid-B

Figure 1: BGA footprint showing arrangement of SMD and NSMD pads for the three different designs.

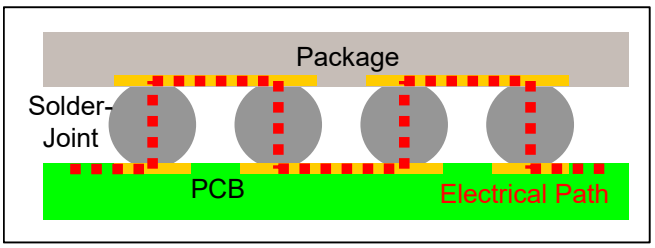


Figure 2: A daisy-chain connection representation between package substrate bottom metal and printed circuit board top metal. The red dashed line illustrates the electrical path.

Table 3: PCB and SMT assembly details.

Parameter	512TEPBGA
PCB Thickness:	1.56mm, 4 layer
PCB Material	FR-4 Epoxy Laminate α1=16ppm/°C E=20GPa Tg=160°C (TMA)
PCB Pad	NSMD, 0.4mm, OSP finish
Stencil	Aperture 0.40mm Thickness 0.10mm
Stencil Finish	Laser cut openings with electropolish and Ni coating
Paste	SAC387 (Sn 3.8Ag 0.7Cu)

Table 4: Experimental matrix.

Cell	Design	Substrate Dielectric Material
1	SMD	Standard
2	Hybrid-A	Standard
3	Hybrid-B	Standard
4	SMD	Low CTE
5	Hybrid-A	Low CTE
6	Hybrid-B	Low CTE

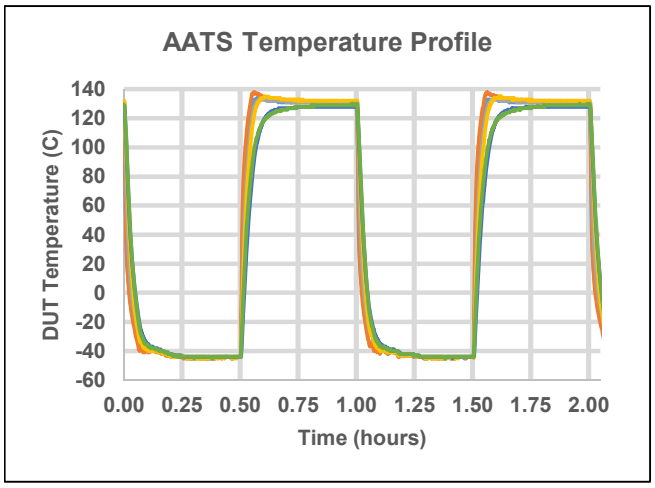


Figure 3: AATS temperature profile.

Cycling, Electrical Testing and Data Analysis
Assemblies were tested in an Air-to-Air Thermal Shock (AATS) dual chamber system whereby one chamber remained hot (+125°C) and the other remained cold (-40°C). An elevator system moved test boards between these chambers within about 10 seconds.

Both chamber dwell times were set at 30 minutes totaling 1 cycle/hour. Typically ~5 minutes was required to reach equilibrium, yielding ~25 min dwells. Figure 3 displays a typical temperature profile obtained by placing thermocouples in the assembly solder-joints.

Assemblies were monitored in-situ during cycling using a 1.2mA current through each net. An event detector logged a failure when a net resistance exceeded 300 ohms. Failures were defined per IPC-9701 [4]. Generally daisy-chain resistances were few ohms at the beginning of an experiment.

Net resistance did not immediately change measurably during early stages of solder-joint crack growth, but climbed quickly as the crack approached 100%. Therefore a net failure was logged when any one of the solder-joints in that net had a crack near 100%.

For each test cell, cycling continued until at least 75% of the samples failed, after which the data were fit to a 2-paramter Weibull distribution using MLE (maximum likelihood estimate). Three metrics of solder-joint lifetime were extracted from each distribution: (1) characteristic life (Eta), (2) extrapolated number of cycles for a 1% failure rate, and (3) first failure. Each of these metrics were linearly regressed versus the DOE factors.

Package Characterization
Solderball height, diameter and coplanarity of the unmounted packages were measured at room temperature using an RVSI LS8000 scanner. Ball height was measured relative to the soldermask surface. The widest portion of the ball was taken as the ball diameter. Coplanarity was calculated according to the seating plane method described in JESD22-B108A [5]. Package warpage was measured using an Akrometrix TherMoire PS400 according to JEDEC standard JESD22-B112A [6], and reported here for the temperature range of interest: -40°C to 125°C. Measurements were made on the bottom (substrate) side of the package after removing the solder spheres.

Crack Propagation Analysis
Two methods were used to examine crack propagation in the solder-joints during cycling: dye-and-pry and cross-section.

Dye-and-pry was a quick and simple method to obtain an overall view of cracking quantity, degree and distribution. A dye was applied to the solder-joint array to in order to mark crack locations, followed by a forced separation of package from board. Cracks formed during cycling were stained with ink, and were distinguishable from fracture surfaces created merely as a result of the forced pry [7].

Dye-and-pry had some limitations. First, it only revealed one crack interface in each solder-joint, whichever cleaved first during pry. Sometimes a solder-joint cracked along both package and PCB sides simultaneously. Additionally, PCB pads often ripped out during peel, even when solder-joint cracking had occurred. In these incidences it was assumed the degree of cracking was low (<50%) since the solder-joint strength was greater than PCB pad adhesion.

For cross-section, standard potting, sectioning, grinding and polishing techniques were used to prepare and study solder-joint crack growth. SEM images were captured for the measurements. In all cases, sections were made through the joint center line. Cross-sections provided a more definitive picture of crack propagation location in the solder-joint than dye-and-pry. Often cross-section identified multiple cracks within a joint. One caution: crack front propagation may be at any arbitrary angle to the cross-section plane, thereby distorting crack length measurements.

Samples were studied for degree of crack growth, location within the solder-joint, and distribution across the array. For solder-joints examined by cross-section, degree of cracking was calculated as the percentage of visible crack length divided by apparent pad diameter (all linear). For dye-and-pry, it was the crack area (red die visible) divided by pad area for each pad where a crack surface was revealed. See Figure 4 as an example.

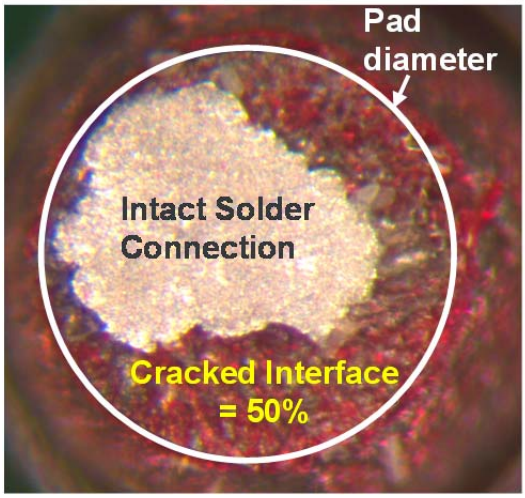


Figure 4: Example dye-and-pry image and degree of cracking calculation.

RESULTS

Ball Size and Coplanarity Characterization

Solder ball diameter and height of the unmounted packages are summarized in Figures 5 and 6, respectively. Distributions for the SMD and NSMD pads are plotted separately. 20 packages were measured for each cell. For both dimensions, the balls on the SMD pads were essentially the same across all the cells. This was expected since these dimensions were dictated by the package substrate SRO and solderball size, which were nominally. Likewise the balls on NSMD pads were the same among the cells.

Since solder wets the NSMD pad sidewalls, it's expected that the height of these pads would be lower than an SMD pad of the same diameter. Surface evolver simulations predicted the NSMD pads would be 22µm shorter if the same 0.45mm pad were used. To compensate, the NSMD pads were designed slightly smaller. Surface evolver predicted only a 3µm difference for the compensated NSMD pads. Figure 6 shows that an actual difference of 6µm was observed. No difference was apparent in ball diameter.

Room temperature solder ball coplanarity is summarized in Figure 7. There is a tendency for the hybrid Cells 2-3 and 5-6 to be slightly higher than the SMD Cells 1 and 4 due to the slight difference in ball heights. Also, the low CTE Cells 4-6 were higher than the standard material Cells 1-3. This was unexpected and is opposite the warpage results shown in the next section. Reasons for this discrepancy are under investigation. In any event, all are well within the Case Outline (Package Outline) specification of 200µm max.

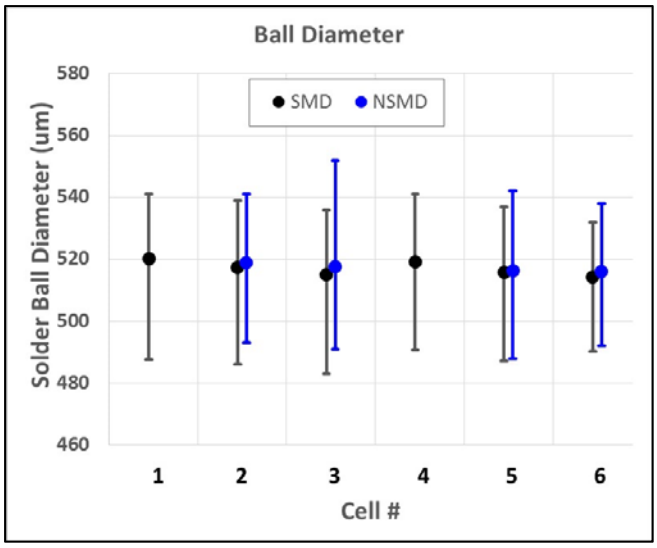


Figure 5: Ball diameter measurement by RVSI scanner. Error bars represent the data range.

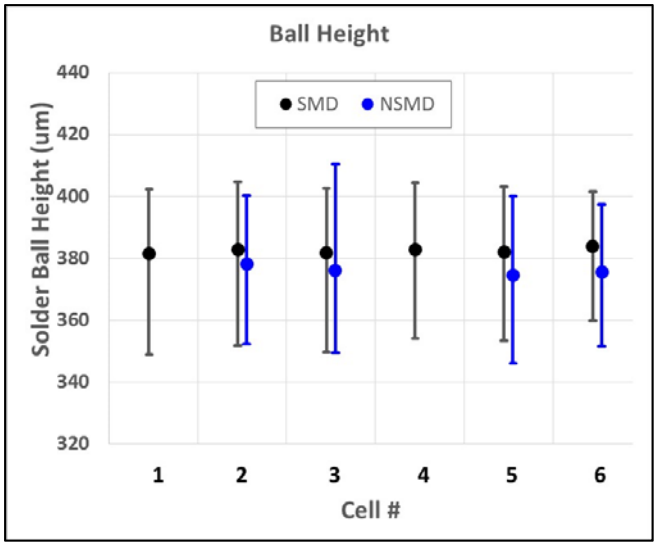


Figure 6: Ball height measurement by RVSI scanner. Error bars represent the data range.

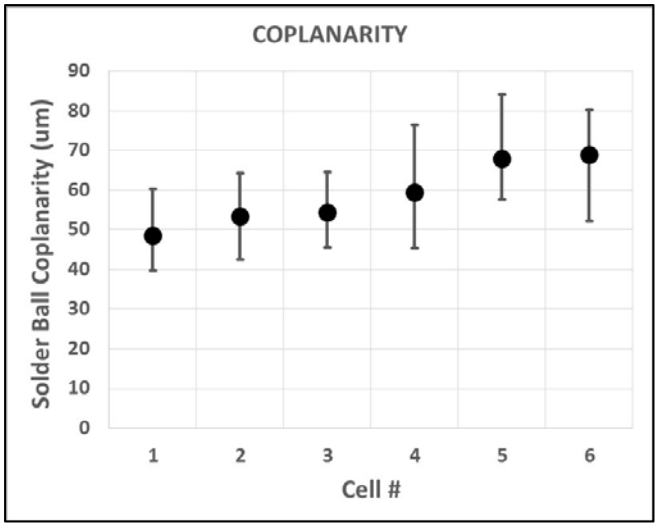


Figure 7: Solder ball coplanarity at room temperature.

Warpage

Figure 8 plots the freestanding component warpage across the thermal cycle temperature range. One sample per cell was measured. Pad design was not expected, nor observed, to influence package warpage. Therefore the three samples for each substrate material type were considered to be from the same populations.

Packages using the low CTE dielectric warped considerably less on the cold side (-40°C to +25°C), 25µm on average. This was expected based on the following analysis. Package warpage is driven primarily by the CTE mismatch between the mold compound and substrate. Below Tg, the mold compound expansion is 9ppm/°C. The low CTE dielectric expansion is 11ppm/°C, but the standard dielectric is 16ppm/°C. Therefore the package will warp as it is cooled from the neutral temperature (roughly 150°C to 175°C.) But since the delta between mold compound and substrate is greater for the standard dielectric, the warpage will also be greater.

Solder-Joint Characterization

One unit from each of two hybrid Cells 2 and 6 were selected for T0 solder-joint characterization after mounting to the PCB. Standoff and solder-joint diameter were measured for 4 joints of each pad type (SMD and NSMD) for each sample. Examples are shown in Figures 9 and 10. Surface evolver predictions based on single joints anticipated the NSMD solder-joints would be about 7µm shorter. However, the actuals were much closer since attaching both types in a single package forces them to a common standoff. The standoff differences observed here between the two types possibly resulted from PCB or package warpage. Overall the joints were shorter and wider than predicted.

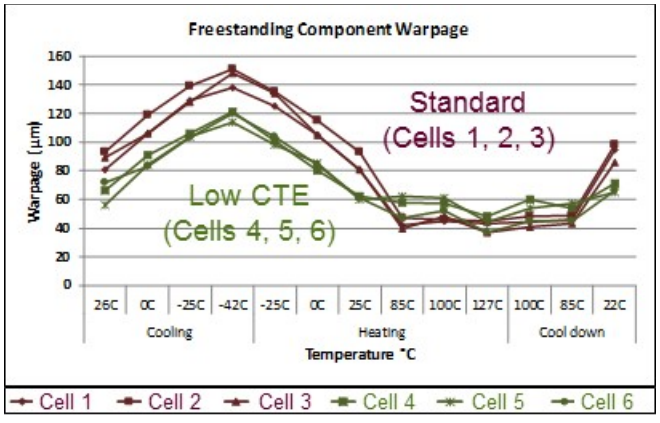


Figure 8: Package warpage by Thermoiré.

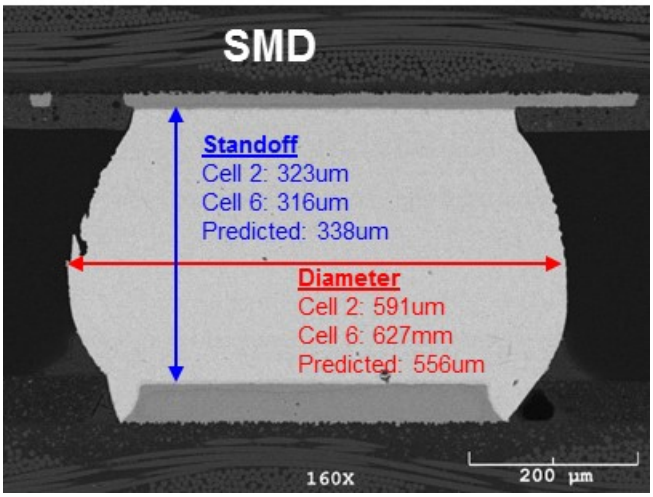


Figure 9: Cross-section of typical SMD solder-joint after mounting to PCB.

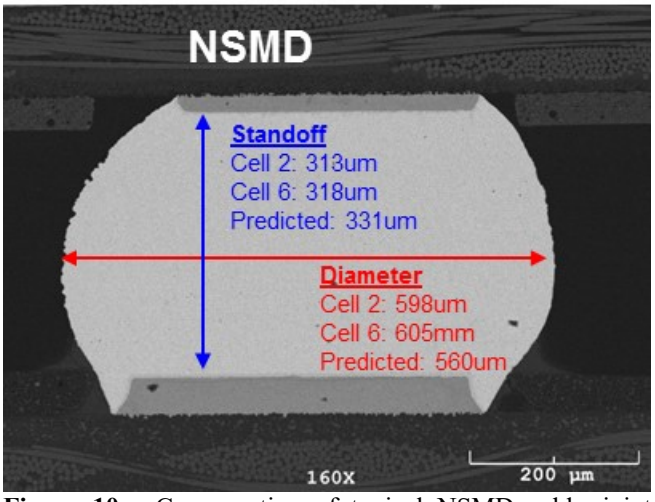


Figure 10: Cross-section of typical NSMD solder-joint after mounting to PCB.

Temperature Cycle Electrical Test Results

Sixteen components from each of the six cells described in Table 4 were mounted on PCBs and cycled -40°C to +125°C as described above. The test was terminated after all cells had at least 12 units fail (75%). The results are plotted in Figure 11. The legend symbol n/s represents the number of units tested (n) and number of suspensions (s). Also shown are the fitted two-parameter Weibull characteristic life (Eta) and shape factor (Beta). Good fits were obtained for all except Cell 1, which had an outlier first failure. Inspection of the graphs suggests that the six populations can be divided into three groups. From least to most reliable: (A) Cell 1; (B) Cells 2,3&4; (C) Cells 5&6. This suggests that the low CTE dielectric or either hybrid design offered an improvement over the baseline, and that combining them was best.

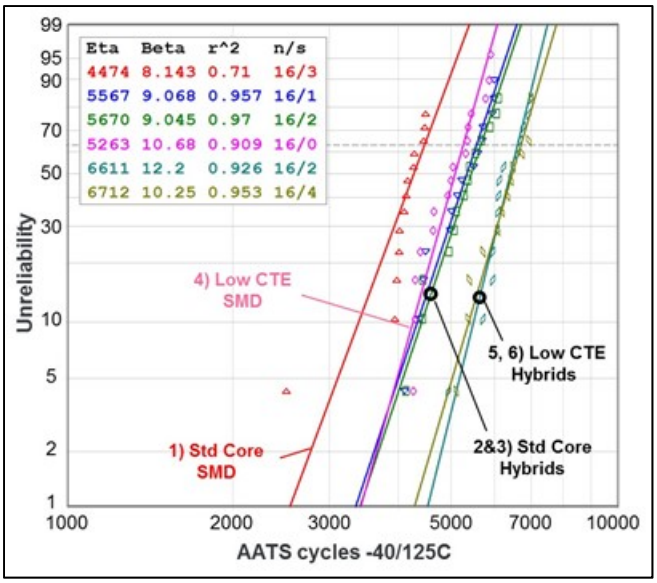


Figure 11: Weibull plot by experimental cell.

Table 5: Summary of Weibull results

Cell	Pad Type	Dielectric Material	Beta	1st Fail	Eta	1% Failure Cycle
1	SMD	Standard	8.1	1st 2499 2nd 3945	4474	2543
2	A	Standard	9.1	4115	5567	3352
3	B	Standard	9.0	4134	5670	3410
4	SMD	Low CTE	10.7	4265	5263	3421
5	A	Low CTE	12.2	4954	6611	4535
6	B	Low CTE	10.3	5113	6712	4285

Three metrics (Eta, extrapolated 1% failure cycle and first failure) were extracted from each distribution and have been summarized in Table 5. Each of these metrics was linearly regressed against the DOE factors to assess impact on solder-joint lifetimes. Results are summarized in Tables 6 and 7 for number of cycles and percentage, respectively. Factors not statistically significant at the alpha=0.05 level are donated with an "*". Each of the three metrics tells the same story. Examining Eta, the low CTE material added nearly 1000 cycles, or 22%, to the solder-joint lifetime. The hybrids added about 1200-1300 cycles, or 30%. In combination, the lifetime was improved over 2200 cycles, ~50%. This statistical analysis confirms the impression from inspection of the Weibull plots.

Cross-Section after Cycling

After 3000 cycles, one unmonitored unit per cell was removed from the chamber for crack growth characterization by cross-section. Each was sequentially cut, polished and imaged by SEM at BGA rows B, F and K. Row B was selected for cross-section analysis since it experienced more significant cracking than row A as discovered during previous investigations [8]. Row K was along the die edge. From Figure 1, note rows B and F were all NSMD for both hybrid designs. Row K was all NSMD for Hybrid-B, but contained both types for Hybrid-A.

Table 6. Change in solder-joint lifetime (# of cycles).

		1st Fail	Eta	1% fail cycles
Dielectric Material	**Standard → Low CTE**	1195	958	979
Design	**SMD → Hybrid-A**	1153	1221	962
	SMD → Hybrid-B	1242	1323	866
	Hybrid-A → Hybrid-B	89*	102*	-96*
Dielectric + Design	**Std + SMD → Low CTE + Hybrid**	2392	2230	1892

* Not statistically significant

Table 7. Change in solder-joint lifetime (%).

		1st Fail	Eta	1% fail cycles
Dielectric Material	**Standard → Low CTE**	43%	22%	39%
Design	**SMD → Hybrid-A**	41%	28%	39%
	SMD → Hybrid-B	45%	30%	35%
	Hybrid-A → Hybrid-B	2%*	2%*	-2%*
Dielectric + Design	**Std + SMD → Low CTE + Hybrid**	86%	51%	76%

* Not statistically significant

The degree of cracking was calculated for each solder-joint as described above. Figure 12 shows a color-coded mapping of the BGA arrays. Red represents joints with over 90% crack length, yellow for those with cracks between 50% and 90%, and green for those with cracks less than 50% of the pad length. Cracks greater than 90% were observed only on the SMD Cells 1 and 4. However, these occurred under the die edge along row K which in principle should behave the same as Hybrid-A for these particular joints. This result also differs from the previous study [8] which found more advanced cracking in row B in the cross-sections. Overall the hybrid cells had less cracking than the SMD cells, matching the electrical test results in this regard.

The solder-joints with the most advanced cracking are presented in Figures 13 and 14. Failure locations within the solder-joints are very typical: in the bulk solder near the interfacial IMC (intermetallic compound), predominantly on the package side, but a few on the PCB side as well. Keep in mind that a solder-joint with 100% linear crack length measured in cross-section would not necessarily fail

electrically, since the sectioning plane may completely miss portions of the solder-joint that are still intact.

Dye-and-Pry after Cycling

At 4013 cycles, dye-and-pry was performed on an unmonitored sample from each of the cells, and degree of cracking calculated. Crack distribution maps are shown in Figure 15 using the same color-coding as above. The patterns here are consistent with the electrical test results. Cell 1 – SMD with standard material – showed the most solder-joints with significant cracking. Only one solder-joint with greater than 50% cracking was observed in the low CTE cells versus 26 for the standard material. While cracking was observed in all portions of the array, the second-to-last ring of joints experience the most. This ring experienced higher strain than the outer-most since the mold cap did not extend to the package edge. This result is consistent with the prior published study, which more fully explains the mechanism [8].

Example images of the dye-and-pry from Cell 1 are shown in Figure 16. The fracture surfaces were between solder ball and package BGA pad, consistent with cross-section.

DISCUSSION

The original hypotheses were (1) a hybrid design with SMD pads under the die and NSMD pads outside the die have longer solder-joint lifetime than a pure SMD design, and (2) low CTE substrate dielectric material would perform better than the standard material. Let's examine each in turn.

It's been long established that NSMD pads reduce strain in the solder-joint [1, 2], offering potential to improve solder-joint lifetime. Our recent investigations on 292MAPBGA and 416PBGA packages also demonstrated slower crack growth on NSMD BGA pads. However these packages failed prematurely due to package side substrate trace cracks [3]. Once it was recognized that this alternate failure mode occurred only in the die shadow, the hybrid designs were created which placed NSMD only on the outer BGA rings.

The hybrid designs outperformed the pure SMD designs in all metrics studied in the current investigation. They had on average approximately 1300 cycles longer characteristic life, and 1200 more cycles to first failure. Less cracking was noted using both dye-and-pry and cross-section.

The manufactureability of mixing pad types on the same package was proven feasible. There were no abnormalities or yield issues reported during assembly of the packages. Ball geometry and coplanarity, while slightly different, were within tolerance. These features can be further fine-tuned with the appropriate choice of relative pad sizes. With package coplanarity well within spec, the change was transparent to board assembly.

One factor not studied was comparison of the hybrid design to a pure NSMD. Perhaps there were facets of this 512TEPBGA package that made it less susceptible to the trace cracking observed on the other packages [1]. The similarity in performance between the two different hybrid designs leaves this an open question. Since Hybrid-A had SMD along the die edge, while Hybrid-B had NSMD, we expected some difference in behavior. Other aspects of the NSMD pads also need exploring, such as the ability to withstand shock from handling and shipping, and performance in drop, shock and vibration testing.

Lowering the substrate dielectric CTE from 16ppm/°C to 11ppm/°C changes the overall mechanics of the package. As noted above, package warpage is driven primarily by the CTE mismatch between the mold compound and substrate. Given the mold compound expansion of 9ppm/°C, the low CTE core is only mismatched by 2ppm/°C, versus 7ppm/°C for the standard material. Therefore at low temperatures the package using a low CTE substrate material should warp less. Though it was not manifest in the room temperature coplanarity data, the TherMoire results clearly show a transition to temperature range where the standard material package is significantly more warped.

Results of the electrical tests were clear: the lower CTE added over 950 cycles to the characteristic life, and nearly 1200 cycles to the first failure. Cross-section and dye-and-pry did not show clear trends. The inconclusiveness of the crack growth data likely resulted from the small sample sizes.

Based on the strength of the electrical test and warpage data, the low CTE substrate dielectric material did perform better. Verification will be needed to confirm the results, ensure it scales across different package types, and to better analyze the crack growth mechanics.

CONCLUSIONS

The conclusions are:

1) A hybrid design, mixing SMD and NSMD pads on the same package is feasible for manufacturing, and was demonstrated to improve the solder-joint characteristic life of a 512TEPBGA package by 30%.
2) Lowering the package substrate dielectric CTE from 16ppm/°C to 11ppm/°C was demonstrated to improve the solder-joint characteristic life of a 512TEPBGA package by 22%
3) Greater than 3000 cycles to first failures for the 512TEPBGA package solder-joint lifetime in -40°C to +125°C TCoB testing.

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APPENDIX

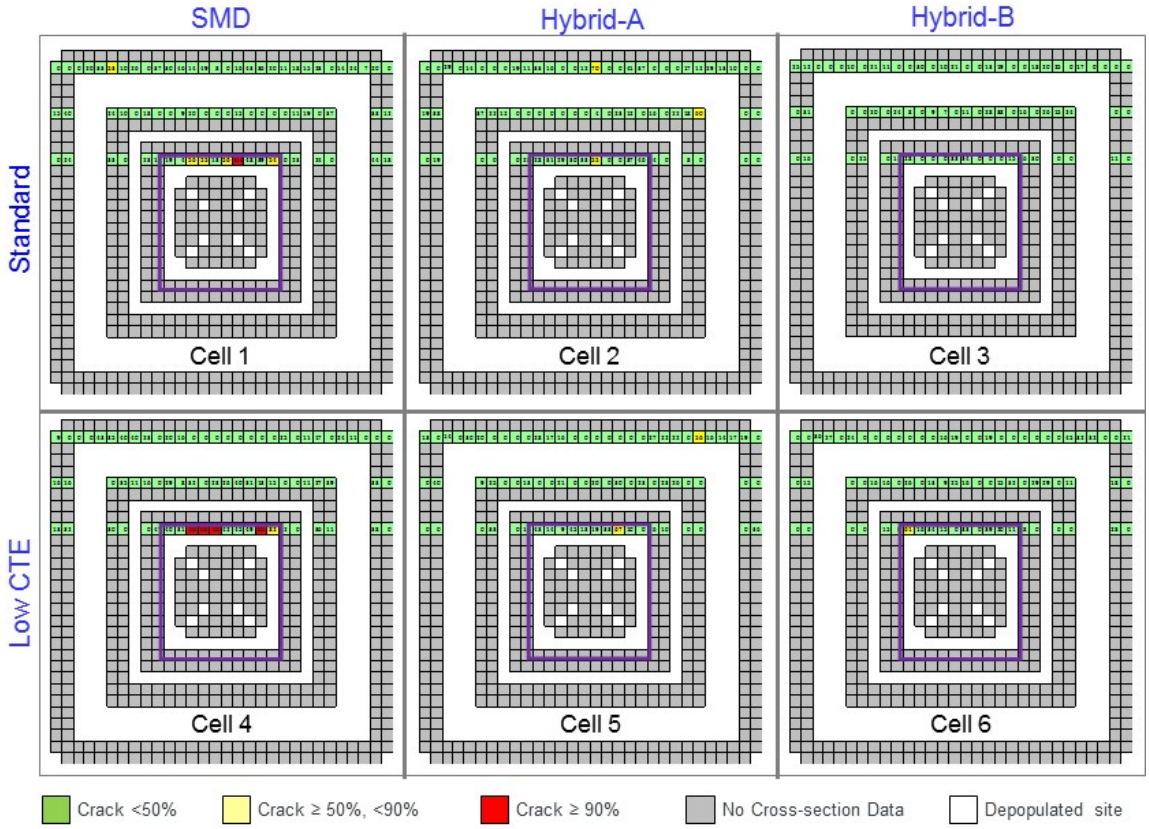

Figure 12: Distribution of degree of crack growth after 3000 cycle, as determined by cross-section.

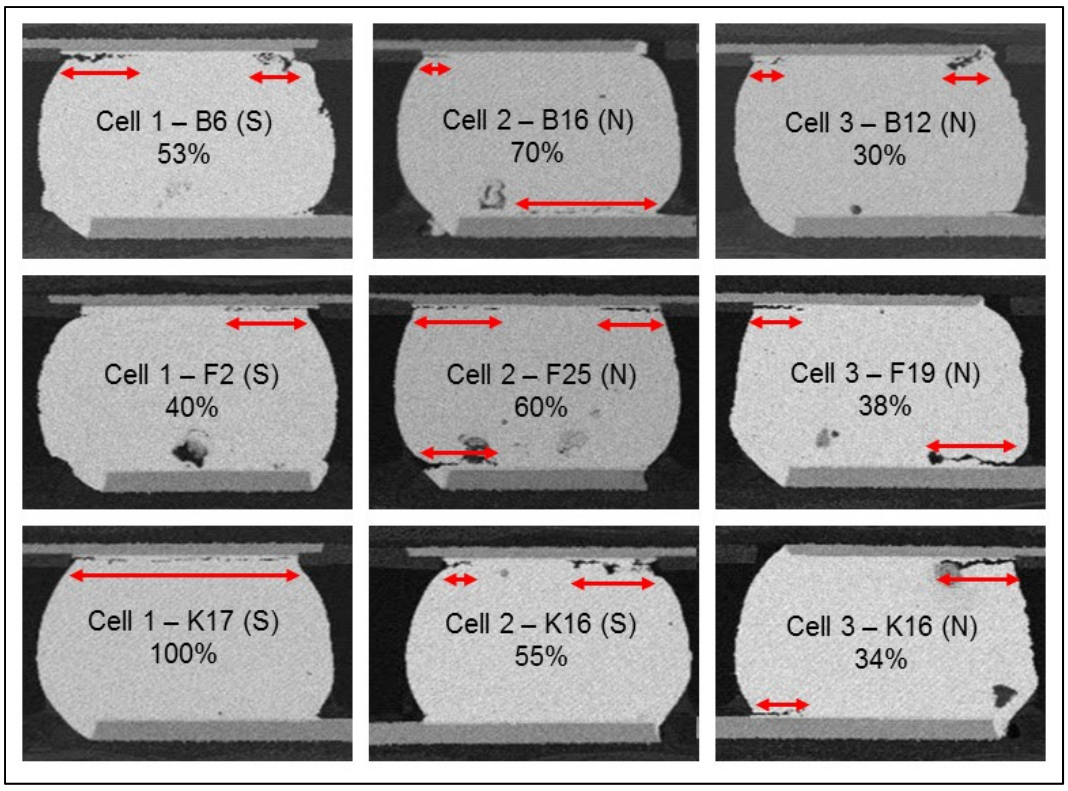

Figure 13: Solder-joints with most advanced crack growth after 3000 cycles from Cells 1-3. Pad type is noted parenthetically.

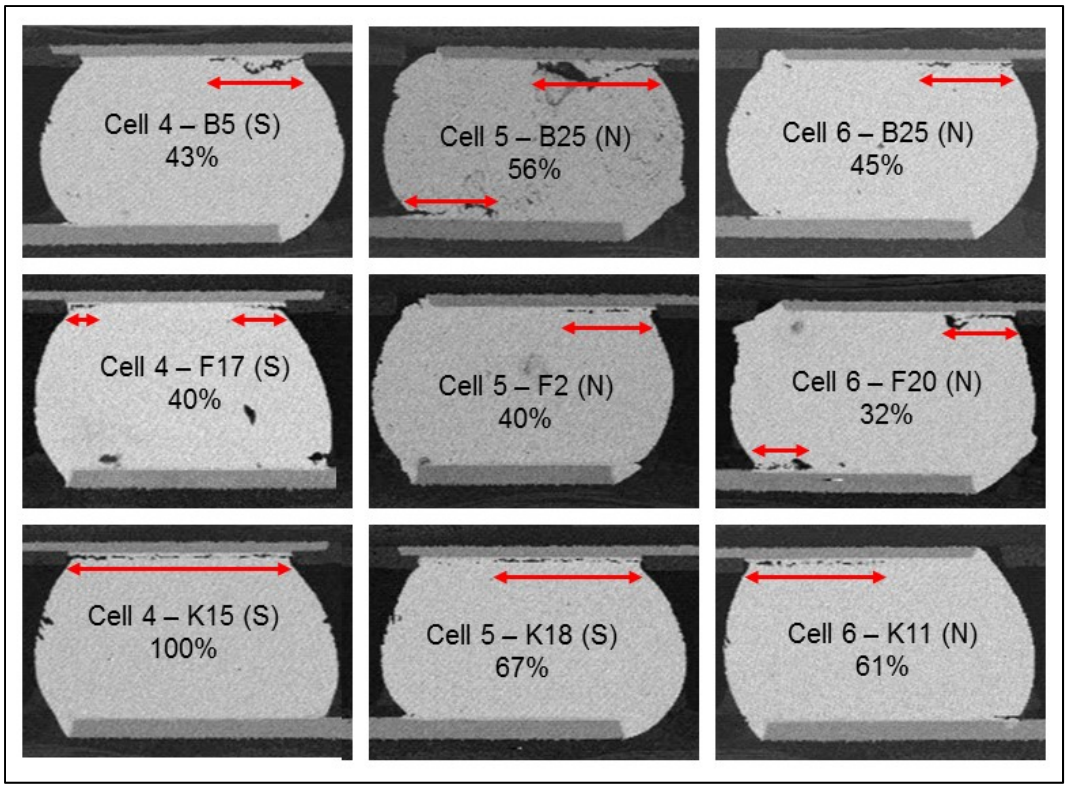

Figure 14: Solder-joints with most advanced crack growth after 3000 cycles from Cells 4-6. Pad type is noted parenthetically.

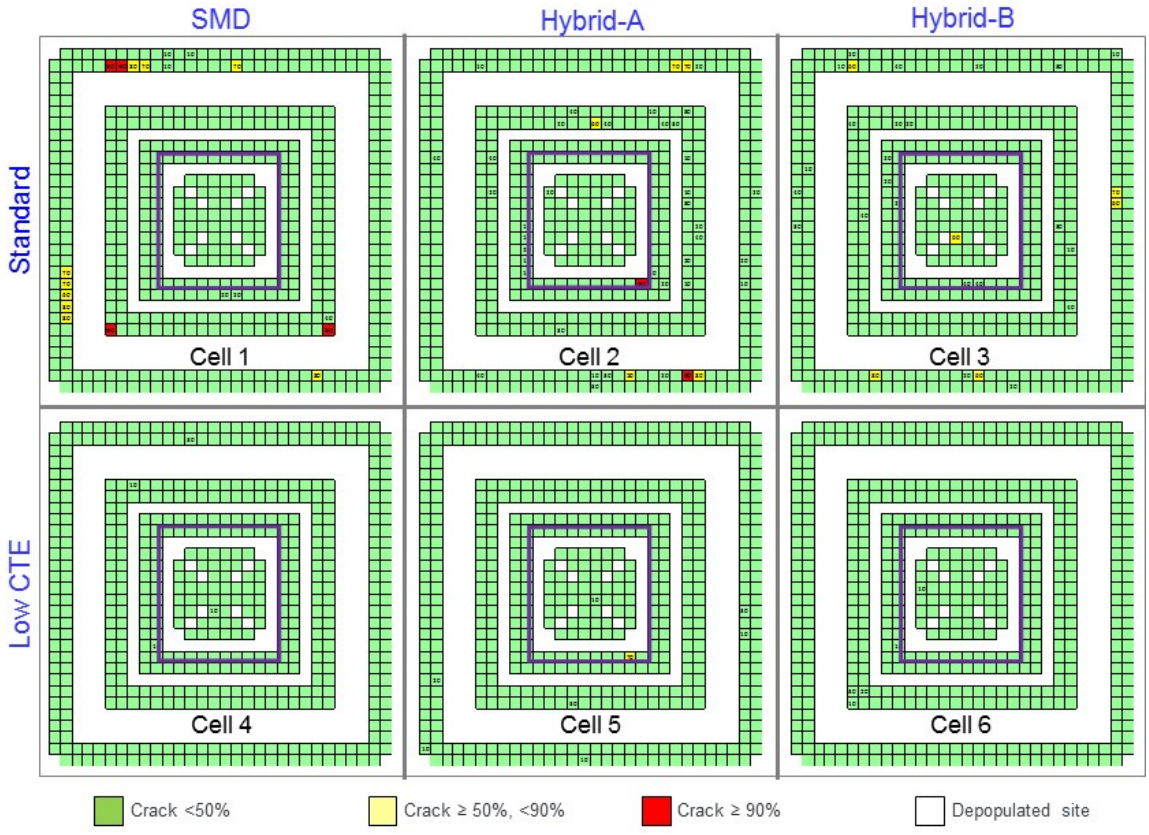

Figure 15: Distribution of degree of crack growth after 4013 cycles, as determined by dye-and-pry.

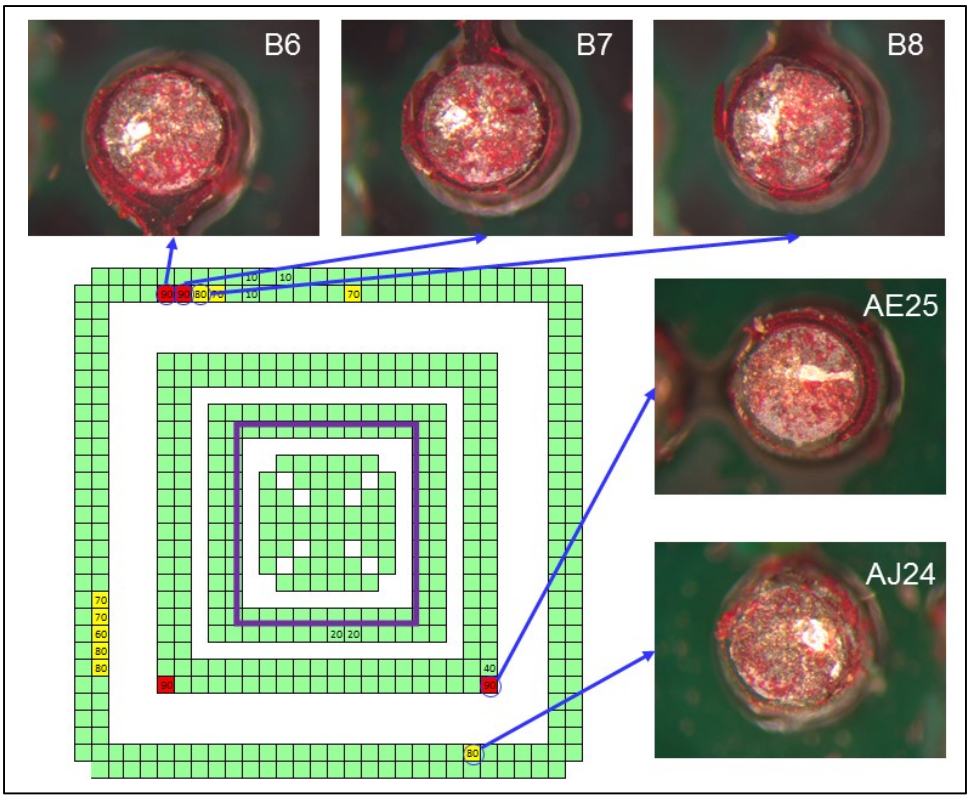

Figure 16: Example dye-and-pry results after 4013 cycles from Cell 1. Images are PCB view, on top of BGA ball attached to PCB pad after pry. Fracture surfaces were between solder ball and package BGA pad. Red area was fractured during cycling. Shinny area was still intact.